Dielectric barriers, pore sealing, and metallization

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Abstract

Future high performance on-chip interconnect requires ultra-low K materials with an effective dielectric constant less than 2.0. Ultra-low K materials normally contain a certain degree of porosity. One of the key issues in the integration of porous materials is the inability of these materials to prevent gaseous penetration during the metallization process such as chemical vapor deposition (CVD) or atomic layer deposition (ALD). In this paper we describe a novel idea to seal the porous ultra-low K film using a thin Parylene layer deposited by a chemical vapor deposition technique. Interaction of metal barrier such as Ta and Ru with Parylene are explored. We found that Ta films deposited on Parylene surface exhibit the desirable alpha phase which has a bcc structure. We also found that Ta does not diffuse into Parylene films under a bias temperature stress of 0.5 MV/cm at 150°C, but Ru does.

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1. Introduction

The research on Cu–low K (K<2.5) technology appears to be much more challenging than anticipated several years ago [1]. A main focus has been to use materials that possess some degree of porosity. Progress has been delayed due to many integration issues [2]. In addition, inferior mechanical stability often leads to poor adhesion, not just in on-chip interconnect, but also at the packaging level. Several non-porous materials with a dielectric constant around 2.2 to 2.3 range do exist [3–5], but less research has been focused on these materials. For dielectric constant around 2, the only non-porous material is the Teflon family [5]. Unfortunately the thermal stability of the Teflon family is not high enough for foreseeable processing requirements. Therefore for K~2, one does not seem to have much choices, either adopt an air-gap technology or live with films with porosity.

Strategies have been proposed to minimize the processing damage to the porous films during etching and ashing [2]. Assuming that this can be achieved with reasonable success, the next step is to seal the pores at the surface, especially at the sidewalls after the trench and via etching [6]. This is to prevent metal or precursor penetration during the metallization process, especially by advanced conformal deposition techniques such as atomic layer deposition. Pore sealing therefore becomes a very important step. There is more than one way that has been proposed to seal the pores at the surface prior to metallization [6]. The sealing of pores is normally accomplished by a dense dielectric layer, the dielectric barrier. Fig. 1 is a schematic showing the necessity of pore sealing prior to metallization in a dual-damascene structure. Some important requirements of this dense dielectric barrier are that it must be by itself a low K material and be able to prevent metal diffusion. From the performance point of view, an ideal case would be to put Cu directly on this dielectric barrier with no metal barrier in between. Unfortunately, even if the dielectric barrier can resist Cu diffusion, Cu normally does not adhere very well to dielectric. If Cu does not bond very well to the dielectric, this would cause electromigration problem when a high current density is passing through the Cu wire. It may therefore be required to use a thin metal layer to serve as an adhesion promoter (and diffusion barrier) between the dielectric barrier and Cu. It is important to recognize that the metal barrier itself should not diffuse into the dielectric.
barrier under the normal integrated circuit processing and operation conditions.

2. Pore sealing by CVD polymer

Here we discuss a particular way to seal the pores at the surface by a chemical vapor deposition technique. We have shown that CVD Parylene (poly(p-xylylene), or PPX) as thin as 3 nm can be used to effectively seal porous MSQ (methyl silsesquixane) films [7]. We call this “Molecular Caulking™ (MC™)” technique. The process involves the sublimation of the precursor paracyclophane at a temperature of 155 °C. The sublimed precursor flies into a high temperature region (650 °C) of the reactor inlet where it is quantitatively cleaved into two p-xylylene monomers by vapor phase pyrolysis. These reactive intermediates are then transported to a room temperature deposition chamber where vapor phase pyrolysis. These reactive intermediates are then transported to a room temperature deposition chamber whereupon condensation, spontaneous polymerization takes place. Linear chains of poly(p-xylylene) with unterminated end groups are formed. Bulk poly(p-xylylene) has a dielectric constant of approximately 2.6 and is lower for thinner films. Normally samples are annealed in Ar/H₂ ambient at 250 °C for 30 min after deposition to remove possible contaminants such as oxygen.

PPX itself slightly penetrates in the porous dielectric but does not appreciably change the effective dielectric constant since PPX is also a low K dielectric. For example, we coated a 5 nm thick of PPX film on a 300 nm MSQ porous film with a dielectric constant of 2.0 and a porosity of 49% (average pore size of 4 nm), the effective dielectric constant is 2.1. The vapor pressure during deposition is 5 mT. The penetration of PPX at the PPX-porous MSQ interface can provide a mechanical interlock between the two materials and would enhance the interface fracture toughness [8] which is a very important issue in the packaging of chips with porous materials. Additional advantages include: (a) PPX does not contain oxygen and it can prevent certain metal from oxidizing at the interface and therefore is stable under thermal and electrical stress [9,10]. (b) PPX deposition is selective in that it would grow on the sidewalls of the porous materials but does not grow (or delay) on the metal surface at the bottom of the trench/via [11]. (c) PPX is thermally stable up to 400 °C. In Fig. 2 we show a schematic of the pore sealing concept.

3. Ta barrier on Parylene surfaces

The interaction of Cu to a polymeric surface such as PPX is weak. Cu–C bond does not exist. Therefore one needs a dielectric or metal barrier layer that can be bonded to PPX on one side and Cu on the other side. Here we consider Ta as the barrier layer. Recently sputter deposition of Ta on a PPX film has been shown to have strong interaction because of the formation of Ta carbide [12]. However, a complication on Ta is that it has two phases, α-Ta which is body-centered-cubic and β-Ta which is tetragonal. These phases have very different properties [13]. The α-Ta has advantages over β-Ta for Cu metallization such as lower resistivity and slightly higher density [14,15]. Generally, the phase formation depends on the deposition parameters (e.g., temperature, ion bombardment, etc.), substrate, and the thickness of the film. (One of the reasons that Ta/TaN stack is used in the conventional barrier scheme is that Ta would form the preferred α-Ta phase when sputter deposited on a TaN surface.) Here we examine the Ta phase formation on Parylene surface.

A 30 nm Ta film was grown by sputter deposition on PPX(120 nm)/Si substrate in a high vacuum system pumped down to a base pressure in the range of 10⁻⁷ Torr. The crystal texture information of the Ta/PPX/Si samples was characterized by X-ray diffraction (XRD) using a Scintag diffractometer with a Cu target operated at 50 kV and 30 mA. The wavelength of the Cu Kα1 X-ray beam was 1.54 Å. The diffractometer was calibrated with respect to the peak positions of a Si calibration standard. The θ–2θ XRD scans were performed at an angular step of 0.01° with a scan rate of 1°/min. Fig. 3 shows the θ–2θ XRD profile of the Ta film deposited on the PPX/Si substrate. It is realized that the Ta film has the α-phase with a dominant (110) texture. The intensity of the β-Ta(002) is insignificant. In addition, Ta films show peak shifts towards to smaller angles from the equilibrium position of α-Ta(002) at 2θ = 38.47°. This kind of peak shift is usually due to the intrinsic compressive

Fig. 1. A schematic showing the necessity of using a dielectric barrier for pore sealing of a porous interlayer dielectric prior to metallization.

Fig. 2. An illustration of possible molecular caulking behavior during deposition onto the connected pore structure of porous MSQ.

Fig. 3. XRD profile of the Ta film deposited on the PPX/Si substrate.
stress originating from the so-called “atomic peening effect” during sputter deposition [16]. Atomic peening occurs when the energetic sputter gas or depositing atoms penetrate into lattice planes, which causes the effective lattice spacing to increase and gives a smaller 20 angle in XRD. The shift is ~0.41° for the as-deposited film. In any case it is clear that the Ta films possess the preferred α-Ta phase which has a lower resistivity.

4. Ta/Parylene stability under bias temperature stress

Another concern is the penetration/diffusion of Ta into the dielectric. Although refractory metal such as Ta is thermally stable at high temperatures, it does not diffuse into dielectric materials under thermal annealing at an elevated temperature compatible with semiconductor processing conditions. However, recently we have shown that even refractory metal such as Ta can diffuse into low K dielectric under a bias temperature stress (BTS) condition [17]. This is because metal can be ionized at the interface and the metal ions can drift into the dielectric under a moderate external field. It is therefore important to test the stability of metal/Parylene stack under BTS conditions.

Parylene films (160 nm thick) were deposited on a p-type Si wafer with 53 nm thermally grown oxide layer (for metal–insulator–semiconductor (MIS) structures). A thermal annealing process was performed in a furnace at 250 °C with Ar–3%H2 gas flow for half hour to remove possible contaminations such as oxygen and hydroxyl group chemically adsorbed on the surface of as-deposited Parylene films. The final film thickness and refractive index were measured using variable-angle spectroscopic ellipsometry (VASE, J.A. Wollam Co., Inc.). Fabrication of the capacitor structure was completed by sputter depositing the top Ta gate metal (20 nm/min deposition rate) through a shadow mask with holes of different sizes. The MIS capacitors were annealed in Ar–3%H2 at 250 °C for 1 h prior to the BTS treatment to eliminate the processing induced interface states such as charge traps or fixed charges at the interfaces between dielectric and the substrate and the dielectric and the metal. BTS C–V measurements were performed using a HP 4280A 1 MHz capacitance meter. The MIS samples were subjected to standard BTS conditions of 0.5 MV/cm or 1 MV/cm at 150 °C and then water-cooled rapidly, with the bias on, to room temperature for C–V measurements. Fig. 4 shows various C–V plots of the MIS capacitors which were subjected to BTS at 150 °C and 0.5 MV/cm for 5, 30, 60, and 90 min in sequence. No flatband voltage shift was observed due to these BTS treatments, indicating no metal-related electrical activity in the dielectric under these conditions.

5. Ru barrier stability under bias temperature stress

Recently Ru has been considered to be a possible barrier material. It has been shown that Cu/Ru films are stable at elevated temperatures [18]. It has been proposed that Ru would replace Ta in the Ta/TaN barrier stack. Since TaN has a high resistivity and would give a high contact resistivity, we ask the question whether Ru can be used as a barrier material directly in contact with Parylene. Here we performed a BTS test to
evaluate the stability of Ru/Parylene interface. A 68 nm thick PPX was chemical vapor deposited on 53 nm thermally oxidized p-type <100> Si to create a Ru/PPX/Si MIS structure. Ru was sputter deposited onto the substrate with a rate of 17 nm/min. A shutter is used to cover the substrate for 3 min in order to pre-sputter clean the Ru target surface. The Ru dots of 1 mm diameter have been deposited on the dielectric samples using a shadow mask. The deposition time was 3 min that resulted in dots with thickness ~51 nm.

BTS C–V measurements were performed under the standard conditions of 0.5 MV/cm and at 150 °C. From the flatband voltage shift shown in Fig. 5, it is evident that Ru does drifts into the Parylene sample under this BTS conditions. It is interesting to note that under the same BTS condition, Cu does not drift into the PPX films [9]. The mechanism of metal drift into dielectrics is not completely understood but has been related to the ionization of the metal at the metal/dielectric interface [17,19].

6. Summary

We discussed the issues of pore sealing for porous interlayer dielectric using a very thin layer of Parylene as the sealant. Parylene is itself a low K dielectric and therefore does not contribute significantly to the overall dielectric constant of the interlayer dielectric. The interaction of metal barriers such as Ta and Ru with Parylene surface was studied. Ta films sputter deposited on Parylene surface exhibit the desirable alpha phase, which has a lower resistivity compared to that of the beta phase. We also showed that Ta/Parylene interface is stable under a standard BTS test conditions at 0.5 MV/cm and 150 °C. For Ru, under the same BTS conditions, we observed a clear ionic penetration into the Parylene films. We conclude that it is not desirable to put Ru in direct contact with the Parylene surface.

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References